REMARKS

In this amendment, several claims have been amended in part to address the objections made in the Office Action, as well as to cover certain desired embodiments of the invention. No new matter has been added. For the reasons given below, the amendments are not needed to overcome the art rejections.

The discussion below follows the order of the issues as they have been raised in the Office Action.

Claim Objections

Claims 1 and 31 were objected to for lacking antecedent basis for the limitation *proportion of the amplitude contributions*. This amendment provides the needed antecedent basis clarification in both claims.

Claim Rejections – 35 U.S.C § 112

Claim 24 stands rejected as being incomplete for allegedly omitting certain structural relationships of elements. In particular, there was a question as to the relationship between the *degenerative mesh circuitry* and the other components in the claim. This issue has been addressed in the amendment here to claim 24. In addition, claim 24 has been amended to recite a particular embodiment of the invention as supported in the specification as filed (thus adding no new matter). Claim 24 now refers to *mesh circuitry coupled between the N amplifier circuits to degenerate the N amplifier circuits*, and where *the phase control circuitry has N amplifier circuits that adjust N current signals in accordance with the N interrelated control signals*. Finally, the *interpolator circuitry is to proportion amplitude contributions of the reference clock phases as a function the N current signals*. This should clarify the relationship between the various elements of claim 24.

Claim Rejections – 35 U.S.C § 102

Claim 1, along with its dependent claims 6-11 stand rejected as being anticipated by U.S. Patent 6,380,783 to Chao et al. ("Chao"). According to the Office Action, Chao discloses Applicants' claimed *degenerative mesh circuitry* in Fig. 5, referencing the Resistor and Vcom. According to the Office Action, this *mesh* regulates the bias current IA and IB. Such an explanation is not persuasive however after taking a closer look at Chao.

Fig. 5 is described in Chao at col. 5 line 18 to col. 6 line 19. None of the discussion in that section refers to the Resistors and Vcom, much less refer to them as providing a degeneration effect on any circuit. Rather, it appears that the pair of Resistors and Vcom only serve to set the common mode level to the input of the comparator 20. See also Fig. 8 of Chao, and col. 6 lines 32-41, which describe a phase interpolator according to another embodiment in which the circuitry is single ended and wherein the multiple phases provided by the comparator 20 represent a comparison between the voltage at single output node 92 and the common mode voltage (Vcom) of the interpolator. This does not teach or suggest that the Resistors used in providing this common mode voltage also act so as to degenerate an amplification circuit. Accordingly, as Chao does not disclose Applicants' claimed *degenerative mesh circuitry*, for at least those reasons, reconsideration and withdraw of the rejection of claim 1 is requested.

Claim Rejections – 35 U.S.C § 103

Independent claim 17, together with its dependent claims 20-23, stand rejected as being obvious over Chao in view of U.S. Patent No. 6,509,773 to Buchwald ("Buchwald"). According to the Office Action, Chao discloses the claimed *receiving an interrelated ramping controlled voltage signal associated with a first phase and a second phase...and proportioning an amplitude contribution of the first and second phases based upon the interrelated control signal*, citing Fig. 1, label 34 and in particular labels D<2:0> in col. 4 lines 1-15. Applicants however disagree with this rejection, because, referring now to

Chao at col. 4 lines 50-53, "the gates of the respective selection transistors 50-55 are connected to input selection **bits** D<2:0> from a selection controller (not shown)." The bits D<2:0> are digital/discrete time signals, not *ramping control voltage signals*. There is no suggestion in either Chao or Buchwald to modify the input selection bits of Chao into Applicants' claimed *interrelated ramping control voltage signals*. Accordingly, reconsideration and withdrawal of the rejection of claim 17 is requested.

Allowed Subject Matter

Although several dependent claims were indicated as being allowable if rewritten in independent form, Applicants have made a good faith effort to explain why the independent claims presented in this amendment are themselves allowable. For instance, with respect to claim 24, this claim has been amended to more clearly recite the relationship between the various elements of the claim and avoid any possible rejection under 35 U.S.C. § 112, second paragraph. Also, independent claim 31 was indicated as allowable if rewritten to overcome the perceived antecedent basis issue-this claim has been so amended.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: August 25, 2006

By _____
Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on August 25, 2006.

_____
Si Vuong *August 25, 2006*